1

2

## **CLAIMS**

1 A self-starting reference circuit for providing a reference electrical characteristic 1. 2 comprising: 3 a current mirror including a first p-channel field effect transistor (FET) and a second pchannel FET configured to supply a reference current across the first FET and a mirrored output 4 current across the second FET, each p-channel FET having a gate, a source and a drain wherein 5 the gates of these FETs are connected, the sources are connected to a power supply, and the drain 6 of the second FET is connected to the gates of these FETs; and 7 a current source including a first n-channel FET which is a low-threshold n-channel FET 8 having a source, a gate and a drain, the gate of the low-threshold FET having a gate threshold 9 10 voltage and being connected to the drain of the first p-channel FET and the drain of the lowthreshold n-channel FET being connected to the drain of the second p-channel FET, the current 11 source further including a reference regulator circuit for receiving the reference current from the 12 drain of the first p-channel transistor and a reference output circuit for receiving the mirrored 13 output current flowing from the source of the first low-threshold n-channel FET and outputting a 14 15 reference electrical characteristic. 2. The self-starting reference circuit of claim 1 wherein the gate threshold voltage is about zero 1. 2 volts. 3. The self-starting reference circuit of claim 1 wherein the gate threshold voltage is slightly 1 2 negative.

16

4. The self-starting reference circuit of claim 1 wherein the circuit is implemented in

complementary metal-oxide semiconductor (CMOS).

- 1 5. The self-starting reference circuit of claim 1 wherein the circuit is implemented in analog
- 2 CMOS.
- 1 6. The self-starting reference circuit of claim 1 wherein the low-threshold FET lacks a positive
- 2 threshold voltage implant.
- 7. The self-starting reference circuit of claim 1 further comprises a second low-threshold n-
- 2 channel FET having a gate, a source and a drain, its drain connected to the drain of the first p-
- 3 channel transistor and to its own gate, its gate connected to the gate of the first low-threshold
- 4 FET, and its source connected to the reference regulator circuit;
- 5 said reference regulator circuit comprises a bipolar junction transistor (BJT) having an
- 6 emitter, a base and a collector, the emitter being coupled to the source of the second low-
- 7 threshold n-channel FET and the collector and base being coupled to a ground; and
- 8 said reference output circuit comprising a resistance coupled between the source of the
- 9 low-threshold transistor and ground.
- 1 8. The self-starting reference circuit of claim 6 wherein the circuit is implemented in Bi-CMOS.
- 1 9. The self-starting reference circuit of claim 1 wherein
- 2 said reference regulator circuit comprises a positive threshold voltage n-channel FET
- 3 having a gate, source and drain, the drain connected to the drain of the first p-channel transistor,
- 4 its gate connected to the source of the low-threshold FET, and its source being coupled to a
- 5 ground; and
- 6 said reference output circuit comprising a resistance coupled between the source of the
- 7 low-threshold transistor and ground.
- 1 10. In a self-starting reference circuit for providing a reference electrical characteristic
- 2 comprising a current mirror including a first p-channel field effect transistor (FET) and a second

p-channel FET configured to supply a reference current across the first FET and a mirrored 3 output current across the second FET, each p-channel FET having a gate, a source and a drain 4 wherein the gates of these FETs are connected, the sources are connected to a power supply, and 5 the drain of the second FET is connected to the gates of these FETs, and a current source 6 including a low-threshold n-channel FET having a source, a gate and a drain, the gate of the low-7 threshold FET being connected to the drain of the first p-channel FET and the drain of the low-8 threshold n-channel FET being connected to the drain of the second p-channel FET, the current 9 source further including a reference regulator circuit for receiving the reference current from the 10 drain of the first p-channel transistor and a reference output circuit for receiving the mirrored 11 output current flowing from the source of the low-threshold n-channel FET and outputting a 12 reference electrical characteristic, a method for operating a self-starting reference circuit 13 14 comprising: 15 the low-threshold FET generating a current across its transistor; 16 generating a voltage across the reference output circuit based on the current; generating a voltage across the reference regulator based on the voltage across the 17 18 reference output circuit; and 19 providing a differential voltage between the power supply and the gates of the p-channel transistors causing forward active operation of the p-channel transistors. 20